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Examiner Tonia Meonske

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Time:

10:01 AM

Date:

From:

June 6, 2007

Client/Matter: STMI01-00056

THIS FAX CONSISTS OF 3 PAGE(S) (INCLUDING THIS COVER SHEET). IF THERE IS A PROBLEM IN RECEIVING THIS FAX, PLEASE CALL (972) 628-3600

U.S. Serial No. 09/751,410, filed December 29, 2000

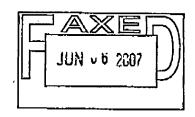
Art Unit: 2181

Ms. Meonske:

Per our telephone conversation, attached is a red-lined copy of the serial nos. for the cross-referenced cases in connection with the above-identified patent application.

Please let me know if you need anything further.

Sincerely, Daniel E. Venglarik



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- 1) Serial No. 09/751,372[Docket No. 00-BN-051],
 filed concurrently herewith, entitled "SYSTEM AND
 METHOD FOR EXECUTING VARIABLE LATENCY LOAD OPERATIONS
 IN A DATA PROCESSOR";
- 2) Serial No. 09/751,331[Docket No. 00-BN-052], filed concurrently herewith, entitled "PROCESSOR PIPELINE STALL APPARATUS AND METHOD OF OPERATION";
- 3) Serial No. 09/751,371 [Docket No. 00-BN-053],
 filed concurrently herewith, entitled "CIRCUIT AND
 METHOD FOR HARDWARE-ASSISTED SOFTWARE FLUSHING OF DATA
 AND INSTRUCTION CACHES";
- 4) Serial No. 09/751,327[Docket No. 00-BN-054],
 filed concurrently herewith, entitled "CIRCUIT AND
 METHOD FOR SUPPORTING MISALIGNED ACCESSES IN THE
 PRESENCE OF SPECULATIVE LOAD INSTRUCTIONS";
- 5) Serial No. 09/751,377 [Docket No. 00-EN-055], filed concurrently herewith, entitled "BYPASS CIRCUITRY FOR USE IN A PIPELINED PROCESSOR;"
- filed concurrently herewith, entitled "SYSTEM AND METHOD FOR ENCODING CONSTANT OPERANDS IN A WIDE ISSUE PROCESSOR";
- 7) Serial No. 09/751,330 [Docket No. 00-BN-058], filed concurrently herewith, entitled "SYSTEM AND

METHOD FOR SUPPORTING PRECISE EXCEPTIONS IN A DATA PROCESSOR HAVING A CLUSTERED ARCHITECTURE";

- Serial No. 09/751,674[Docket No. 00-BN-059],
 filed concurrently herewith, entitled "CIRCUIT AND
 METHOD FOR INSTRUCTION COMPRESSION AND DISPERSAL IN
 WIDE-ISSUE PROCESSORS";
- 9) Serial No. 09/751,678[Docket No. 00 EN-066],
 filed concurrently herewith, entitled "SYSTEM AND
 METHOD FOR REDUCING POWER CONSUMPTION IN A DATA
 PROCESSOR HAVING A CLUSTERED ARCHITECTURE;" and
- 10) Serial No. 09/751,679[Docket No. 00-EN-067],
 filed concurrently herewith, entitled "INSTRUCTION
 FETCH APPARATUS FOR WIDE ISSUE PROCESSORS AND METHOD
 OF OPERATION."